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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/592,207	06/13/2000	Padma S. Nagarasa	00325.00355	7415

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2185	2

DATE MAILED: 03/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/592,207	NAGARASA ET AL.
	Examiner	Art Unit
	Albert Wang	2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: . .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: misspelling of "HSTL" on page 5.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Moloney et al., U.S. Patent No. 5,670,904 (hereinafter "Moloney").

As per claim 1, Moloney discloses an apparatus (Fig. 2, Col. 1 lines 47-67) comprising:

a first delay circuit configured to present a data delayed signal having one of a plurality of delay times , wherein said plurality of delay times provide a user configurable setup/hold time.

As per claims 11 and 12, since Moloney discloses the first delay circuit of claim 1, Moloney discloses the claimed apparatus and method.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 3, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moloney as applied to claims 1 and 12 above, and further in view of Brown, U.S. Patent No. 6,310,506.

As per claim 2, Moloney as applied to claim 1 above does not expressly teach the apparatus further comprising:

a second circuit configured to receive said data delayed signal and present a data output. While not expressly taught, a second circuit is typically used with apparatus such as Moloney's since without a second circuit, the data delayed signal, which is digital, would by undefined. Brown teaches a second circuit (Fig. 1B, input buffer 3 and latch 11) in conjunction with a first delayed circuit (delay network 5). Moloney and Brown are analogous art because they are from the same field of endeavor involving programmable delay circuits. At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Brown's second circuit to Moloney's apparatus in order to maintain the viability of the data signal.

As per claim 3, Brown teaches said second circuit comprises a register that is further configured in response to a clock signal (Fig. 1B, latch signal).

As per claims 13 and 14, since Moloney/Brown teaches the second circuit of claims 2 and 3, the combination teaches the claimed method.

4. Claims 4-10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moloney as applied to claims 1 and 12 above, and further in view of JEDEC Standard No. 8-6, "High Speed Transceiver Logic (HSTL) - A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits", EIA/JESD8-6, August 1995 (hereinafter "JEDEC8-6").

As per claim 4, while Moloney teaches presenting a first signal in response to a data input, Moloney does not expressly teach that said first delay circuit further comprises an HSTL circuit. HSTL is one of multiple transmission logic specifications in common use. It would have been a matter of design to have the first delayed circuit conform to JEDEC8-6 standard. Therefore at the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the JEDEC8-6 standard to Moloney's apparatus.

As per claim 5, Moloney teaches a number of delay circuits (Fig. 2, delay elements 11).

As per claim 6, Moloney teaches a switch (multiplexer 12).

As per claim 7, Moloney teaches a user configuration signal (digital selection signal M).

As per claim 8, Moloney teaches said user configuration signal for selecting a delay which is inherently for setup and hold timing.

As per claims 9 and 10, Moloney teaches said user configuration signal comprises a programmable multi-bit signal (Abstract).

As per claims 15-20, since Moloney/JEDEC8-6 teaches the apparatus of claims 4-10, the combination teaches the claimed method.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

IBM Technical Disclosure Bulletin, "Programmable Delay Line Control Signal Circuits", Vol. 37, No. 8, pp. 519-520, August 1994.

Tsunemoto, Japanese Patent No. 63-177610.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

aw
March 20, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100